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Applicants: David W. Boerstler et al.

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**LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANTS' INFORMATION DISCLOSURE
STATEMENT**

Reference Designation

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
AAA						
ABA						
ACA						
ADA						
AEA						
AFA						
AGA						
AHA						

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes No
AIA						
AJA						
AKA						
ALA						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial

WW AMA Joonsuk Lee et al., "A Low-Noise Fast-Lock Phase-Locked Loop with Adaptive Bandwidth Control," *IEEE Journal of Solid-State Circuits*, Vol. 35, No. 8, August 2000, pp. 1137-1145.

WW ANA Gyoung-Tae Roh et al., "Optimum Phase-Acquisition Technique for Charge-Pump PLL," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, Vol. 44, No. 9, September 1997, pp. 729-740.

WW AOA Masayuki Mizuno et al., "CMOS Hot-Standby Phase-Locked Loop Using a Noise-Immune Adaptive-Gain Voltage-Controlled Oscillator," *1995 IEEE International Solid-State Circuits Conference*, pp. 268-270.

WW APA Rafael Fried et al., "Low-Power Digital PLL with One Cycle Frequency Lock-In Time and Large Frequency-Multiplication Factor for Advanced Power Management," *ICECS '96*, pp. 1166-1169.

WW AQA Helmuth Brugel et al., "Variable Bandwidth DPLL Bit Synchronizer with Rapid Acquisition Implemented as a Finite State Machine," *IEEE Transactions on Communications*, Vol. 42, No. 9, September 1994, pp. 2751-2759.

____ ARA

Examiner:

Date Considered:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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